ELEG 309 - Example Problems Chapter 7-3

**Exercise 7.21**

A CS amplifier utilizes a MOSFET biased at *ID* = 0.25 mA with *VOV* = 0.25 V and *RD* = 20 k. The amplifier is fed with a signal source having *R*sig = 100k, and a 20-k load is connected to the output. Find *R*in, *Avo*, *Ro*, *Av*, and *Gv*. If, to maintain reasonable linearity, the peak of the input sine-wave signal is limited to 10% of 2*VOV*, what is the peak of the sine-wave voltage at the output?

**Example 7.8**

A CE amplifier utilizes a BJT with *β* = 100 is biased at *IC* = 1 mA and has a collector resistance *RC* = 5k. Find *R*in, *Ro*, and *Avo*. If the amplifier is fed with a signal source having a resistance of 5 k, and a load resistance *RL* =5 k is connected to the output terminal, find the resulting *Av* and *Gv*. If π is to be limited to 5 mV, what are the corresponding sig and *o* with the load connected?

**Example 7.9**

For the CE amplifier specified in Example 7.8, what value of *Re* is needed to raise *R*in to a value four times that of *R*sig? With *Re* included, find *Avo*, *Ro*, *Av*, and *Gv*. Also, if π is to be limited to 5 mV, what are the corresponding sig and *o*?

**Exercise 7.25**

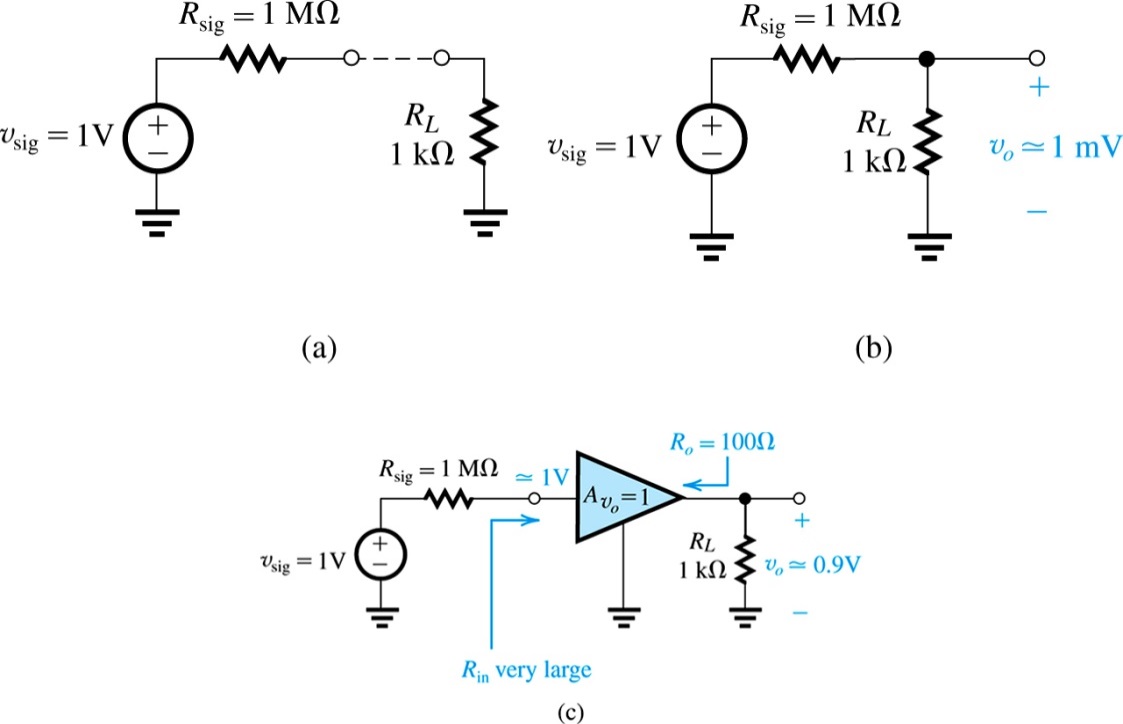
A CG amplifier is required to match a signal source with *R*sig = 100 . At what current *ID* should the MOSFET be biased if it is operated at an overdrive voltage of 0.20 V? If the total resistance in the drain circuit is 2 k, what overall voltage gain is realized?

**Exercise 7.26**

Consider a CB amplifier utilizing a BJT biased at *IC* = 1 mA and with *RC* = 5 k. Determine *R*in, *Avo*, and *Ro*. If the amplifier is loaded in *RL* = 5 k, what value of *Av* results? What *Gv* is obtained if *R*sig = 5 k?

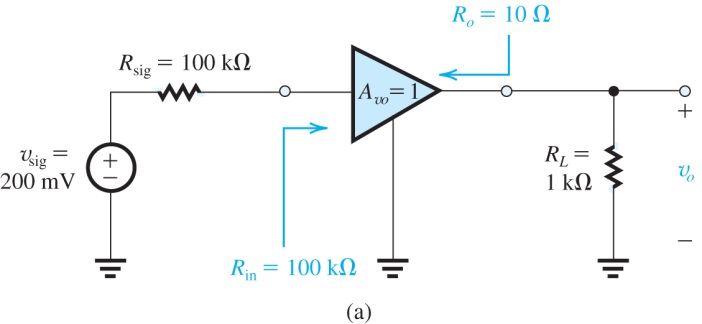
**Exercise 7.28**

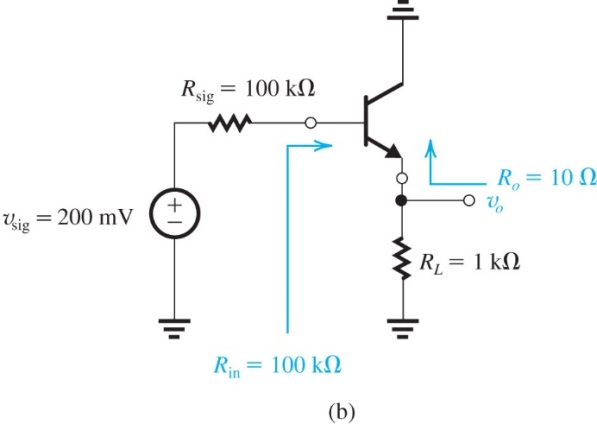
It is required to design a source follower that implements the buffer amplifier shown in Fig. 7.41(c). If the MOSFET is operated with an overdrive voltage *VOV* = 0.25 V, at what drain current should it be biased? Find the output signal amplitude and the signal amplitude between gate and source.



**Example 7.10**

It is required to design an emitter follower to implement the buffer amplifier of Fig. 7.46(a). Specify the required bias current *IE* and the minimum value the transistor *β* must have. Determine the maximum allowed value of *v*sig if *vπ* is to be limited to 5 mV in order to obtain reasonably linear operation. With *v*sig = 200 mV, determine the signal voltage at the output if *RL* is changed to 2 k, and to 0.5 k.





**Figure 7.46** Circuit for Example 7.10.